IN THE CLAIMS

1 (Previously Presented). A method comprising:

providing a register accessible by a plurality of central processing units; and

indicating whether data in said register is available for a given central processing unit by providing different indicators assigned to each of a plurality of central processing units and enabling the given central processing unit to reset its indicator when the data in said register is no longer useful to the given central processing unit.

2 (Previously Presented). The method of claim 1 including indicating for each of a plurality of central processing units whether the data is available for a given central processing unit.

3 (Previously Presented). The method of claim 2 including requiring a central processing unit to wait to execute an instruction until the data it needs to execute the instruction is available in one or more registers.

4 (Previously Presented). The method of claim 3 including providing a bit for each item of data indicating whether a given central processing unit can access that data.

5 (Previously Presented). The method of claim 4 including resetting said bit when said data is accessed by a given central processing unit.

6 (Previously Presented). The method of claim 1 including preventing any central processing unit from writing data to said register until all of the indicators for the plurality of central processing units indicate that the data is no longer useful to any other central processing unit.

7 (Previously Presented). The method of claim 6 including indicating the central processing unit which will utilize the data written into the register.

8 (Previously Presented). The method of claim 1 includes enabling a plurality of central processing units to access a register at the same time.

9 (Previously Presented). The method of claim 1 including providing specialized central processing units for mathematical operations and for memory.

10 (Previously Presented). The method of claim 1 including providing an input central processing unit, an output central processing unit and coupling said input, output and specialized central processing units to said register through a cross-bar connection.

11 (Previously Presented). A computer readable medium storing instructions that, if executed, enable a processor-based system to:

make a register accessible by a plurality of central processing units in said system;

provide different indictors for each of a plurality of central processing units;

indicate whether data in said register is available for a given processing unit; and

enable the given central processing unit to reset its indicator when data in the register is no longer useful for the given central processing unit.

12 (Previously Presented). The medium of claim 11 further storing instructions that enable the processor-based system to determine whether data is available in a register for a particular processing unit.

13 (Previously Presented). The medium of claim 12 further storing instructions that enable the processor-based system to prevent execution of an instruction until the data needed to execute the instruction is available in one or more registers.

14 (Previously Presented). The medium of claim 13 further storing instructions that enable the processor-based system to check a bit in said register for each item of data indicating whether a processing unit can access said data.

15 (Previously Presented). The medium of claim 14 further storing instructions that enable the processor-based system to reset said bit when said data is accessed by a processing unit.

16 (Previously Presented). The medium of claim 15 further storing instructions that enable the processor-based system to avoid writing said data to said register until all the bits indicate that the data is no longer useful to any other processing unit.

17 (Previously Presented). The medium of claim 16 further storing instructions that enable the processor-based system to indicate which processing unit will utilize the data written into the register by another processing unit.

Claims 18-30 (Canceled).